ACS APPLIED MATERIALS & INTERFACES
Research Article
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Surface Passivation and Interface Properties of Bulk GaAs and Epitaxial-GaAs/Ge Using Atomic Layer Deposited TiAlO Alloy Dielectric

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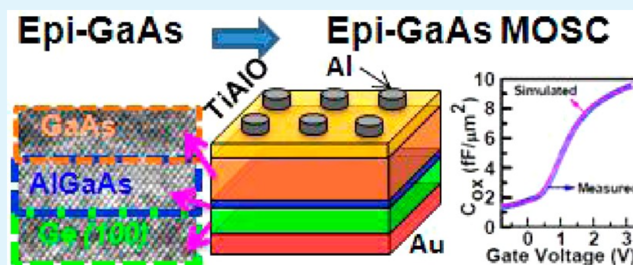

ABSTRACT: High quality surface passivation on bulk-GaAs substrates and epitaxial-GaAs/Ge (epi-GaAs) layers were achieved by using atomic layer deposited (ALD) titanium aluminum oxide (TiAlO) alloy dielectric. The TiAlO alloy dielectric suppresses the formation of defective native oxide on GaAs layers. X-ray photoelectron spectroscopy (XPS) analysis shows interfacial arsenic oxide (As_xO_y) and elemental arsenic (As) were completely removed from the GaAs surface. Energy dispersive X-ray diffraction (EDX) analysis and secondary ion mass spectroscopy (SIMS) analysis showed that TiAlO dielectric is an effective barrier layer for reducing the out-diffusion of elemental atoms, enhancing the electrical properties of bulk-GaAs based metal-oxide-semiconductor (MOS) devices. Moreover, ALD TiAlO alloy dielectric on epi-GaAs with AlGaAs buffer layer realized smooth interface between epi-GaAs layers and TiAlO dielectric, yielding a high quality surface passivation on epi-GaAs layers, much sought-after for high-speed transistor applications on a silicon platform. Presence of a thin AlGaAs buffer layer between epi-GaAs and Ge substrates improved interface quality and gate dielectric quality through the reduction of interfacial layer formation (Ga_xO_y) and suppression of elemental out-diffusion (Ga and As). The AlGaAs buffer layer and TiAlO dielectric play a key role to suppress the roughening, interfacial layer formation, and impurity diffusion into the dielectric, which in turn largely enhances the electrical property of the epi-GaAs MOS devices.

KEYWORDS: *III−V surface passivation, atomic layer deposition, TiAlO alloy dielectric, epi-GaAs/Ge, effective dielectric constant, hysteresis voltage, elemental out-diffusion, GaAs MOS*

INTRODUCTION

Development of epitaxial III−V high mobility channel materials on a silicon (Si) platform is much sought-after to realize complementary metal oxide semiconductor (CMOS) devices with increased carrier mobility and device flexibility.[1−4] Gallium-arsenide (GaAs) and germanium (Ge) have received much attention in this respect due to their lower effective mass and hence intrinsic superior transport property than Si.[4] It is also possible to grow epitaxial GaAs (epi-GaAs) on Ge substrate to realize high performance, flexibility, and enhanced functionality of III−V compounds coupled with the low manufacturing cost and sheer scale of the silicon process.[1−5] For an example, Liu et al. demonstrated long-wavelength InAs/GaAs quantum-dot laser diode monolithically grown on Ge substrate.[5] Performance gains using an epitaxial layer as a channel material are still challenging due to the deleterious effects from the surface roughness and poor interface quality between the epitaxial layer and gate dielectric. The loss of carrier recombination at the surface and interface of GaAs/gate dielectric not only degrades the characteristics of minority-carrier injection devices but also reduces the device lifetime, due to the presence of poor quality native oxide. Therefore, development of high-quality interface with an epi-GaAs channel material is among the most challenging problems in modern semiconductor technology.[1−4]

Even though several approaches had been made to realize high quality interface on bulk-GaAs substrates using high permittivity (high-*k*) dielectrics and interfacial passivation

Received: November 7, 2012
Accepted: January 18, 2013
Published: January 18, 2013

 © 2013 American Chemical Society dx.doi.org/10.1021/am302537b | ACS Appl. Mater. Interfaces 2013, 5, 949−957

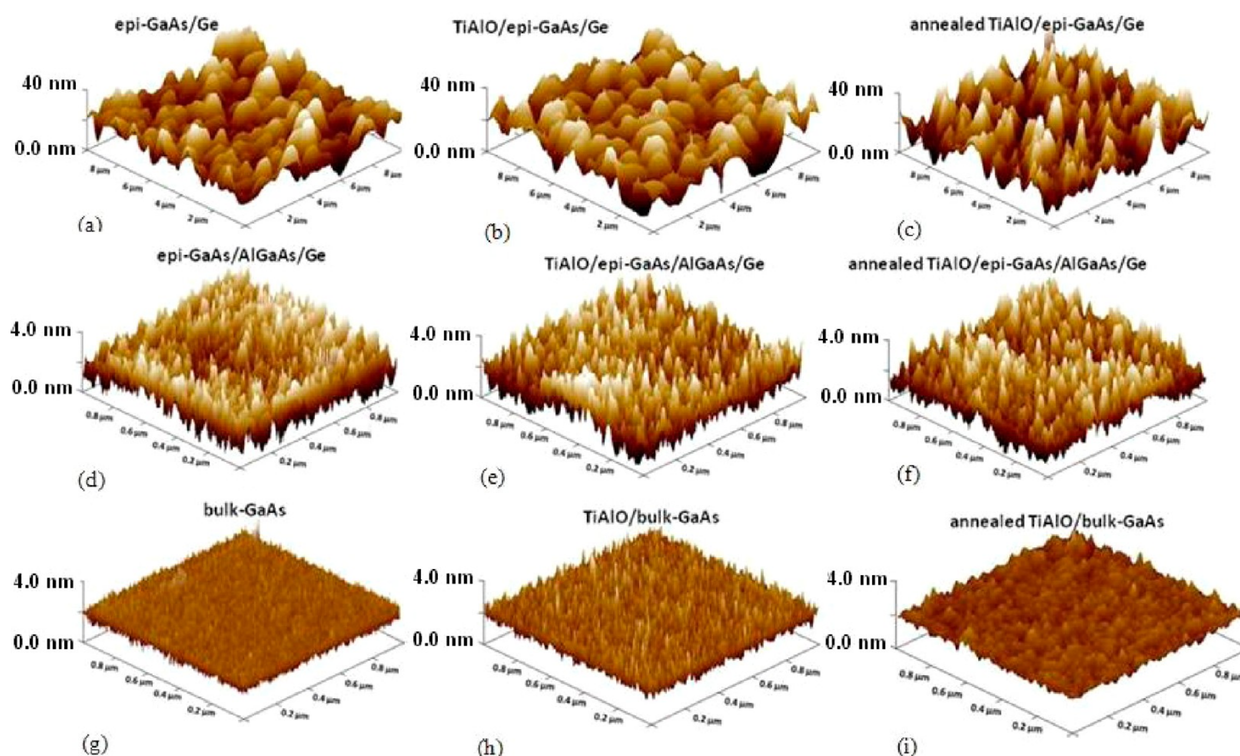

Figure 1. (a) Surface morphology of epi-GaAs layers grown on Ge substrates: (b) after ALD coated TiAlO dielectric and (c) postdeposition annealing (PDA) of TiAlO at 500 °C. (d) Surface morphology of epi-GaAs layers grown on Ge substrates with AlGaAs buffer layer between Ge substrates and epi-GaAs layers: (e) after ALD coated TiAlO and (f) after PDA. AFM images of (g) bulk-GaAs, (h) ALD TiAlO deposition on bulk-GaAs substrates, and (i) after PDA at 500 °C.

layers (IPL),[6−16] there have been continuous efforts to improve the interface quality further. In addition, it is necessary to find the suitable dielectric which is also compatible with germanium substrates. For directly deposited high-*k* dielectric on GaAs substrates, large interface defects and high hysteresis voltage in capacitance−voltage characteristics were observed. Much effort will be needed to improve the interface quality between epi-GaAs and high-*k* dielectrics. The epi-GaAs has unusually high surface roughness (∼5 nm) compared with bulk-GaAs substrates and conventional Si substrates (∼0.3 nm).[17] This leads to the formation of thick defective native oxides; as a result, the electrical properties of MOS devices degraded.[6,17,18] It is well-known that the atomic layer deposited (ALD) dielectrics offer a unique opportunity to passivate bulk-GaAs and epi-GaAs layers using high-*k* dielectrics.[6,11−16,19] In particular, ALD is very crucial for epi-GaAs systems compared to the other deposition technique, since it provides better interface between epi-GaAs and dielectric through conformal coating of the epi-GaAs layers.[14] Even though the ALD HfO_2 and Al_2O_3/TiO_2 dielectrics on epi-GaAs show promising results, the frequency dispersion and hysteresis voltage in $C-V$ characteristics are high.[14,15] The alloy dielectric of Al_2O_3 and TiO_2 (TiAlO) is a very promising dielectric due to its high dielectric constant and high thermal stability.[20] It has been mainly studied for Si- and Ge-based devices for high-*k* gate stacks,[20−22] while there is considerably less work related to the surface passivation of GaAs using TiAlO dielectric.[23,24] In the present work, we have investigated the surface passivation of bulk GaAs substrates and epi-GaAs layer using TiAlO gate dielectric. Gate dielectric quality and interfacial layer formation between TiAlO/GaAs have been discussed in detailed by using X-ray photoelectron spectroscopy (XPS) and secondary ion mass spectroscopy (SIMS). The elemental out-diffusion of Ga and As into TiAlO dielectric was studied using high-resolution transmission electron microscopy (HR-TEM) analysis and electrical properties. In addition, we have also simulated capacitance−voltage ($C-V$) characteristic and compared them with experimental results to determine the interfacial layer thickness and dielectric constant of the interfacial layer.

■ EXPERIMENTAL SECTION

A thin layer of TiAlO dielectric (∼14 nm) was deposited on the epi-GaAs layer and bulk-GaAs substrates. The epi-GaAs are grown at 675 °C by using the metal−organic chemical-vapor-deposition (MOCVD) technique on Ge(100) substrates with 6° off-cut toward the (111) plane. The surface native oxide of Ge substrate was removed at 720 °C in H_2 ambient. After that, the temperature is ramped down to 675 °C to grow a thin AlGaAs (10 nm) buffer layer on the Ge substrates. AsH_3, TMGa, and TMAl are introduced into the reactor for the growth of the AlGaAs buffer layer and 500 nm thick epi-GaAs layer. The details of the epi-GaAs layer that was grown can be found in ref 17. Prior to the deposition of ALD TiAlO dielectric, the as-grown epi-GaAs layers and bulk p-type GaAs substrates are degreased using isopropanol, cleaned in HF solution (1%) for 3 min, and then dipped in NH_4OH solution for 10 min. Thin TiAlO films are deposited using alternative cycles of ALD of Al_2O_3 and TiO_2 with a starting layer of Al_2O_3. Al_2O_3 is deposited on epi-GaAs and bulk-GaAs using trimethylaluminium (TMA, SAFC Hitech, 99.9%) and H_2O as the precursors in viscous flow type (0.6 Torr working pressure) ALD equipment with a N_2 flow rate of 50 sccm at 170 °C. Vapors of $TiCl_4$ (Merck, 99%) and H_2O precursors are sequentially introduced into the chamber for the TiO_2 deposition. For XPS analysis, a TiAlO thin film of ∼5 nm thickness was deposited on bulk-GaAs and the epi-GaAs layer using the same process recipe. Postdeposition annealing (PDA) was carried out in a N_2 ambient at 500 °C for 1 min by rapid thermal annealing (RTA) technique.

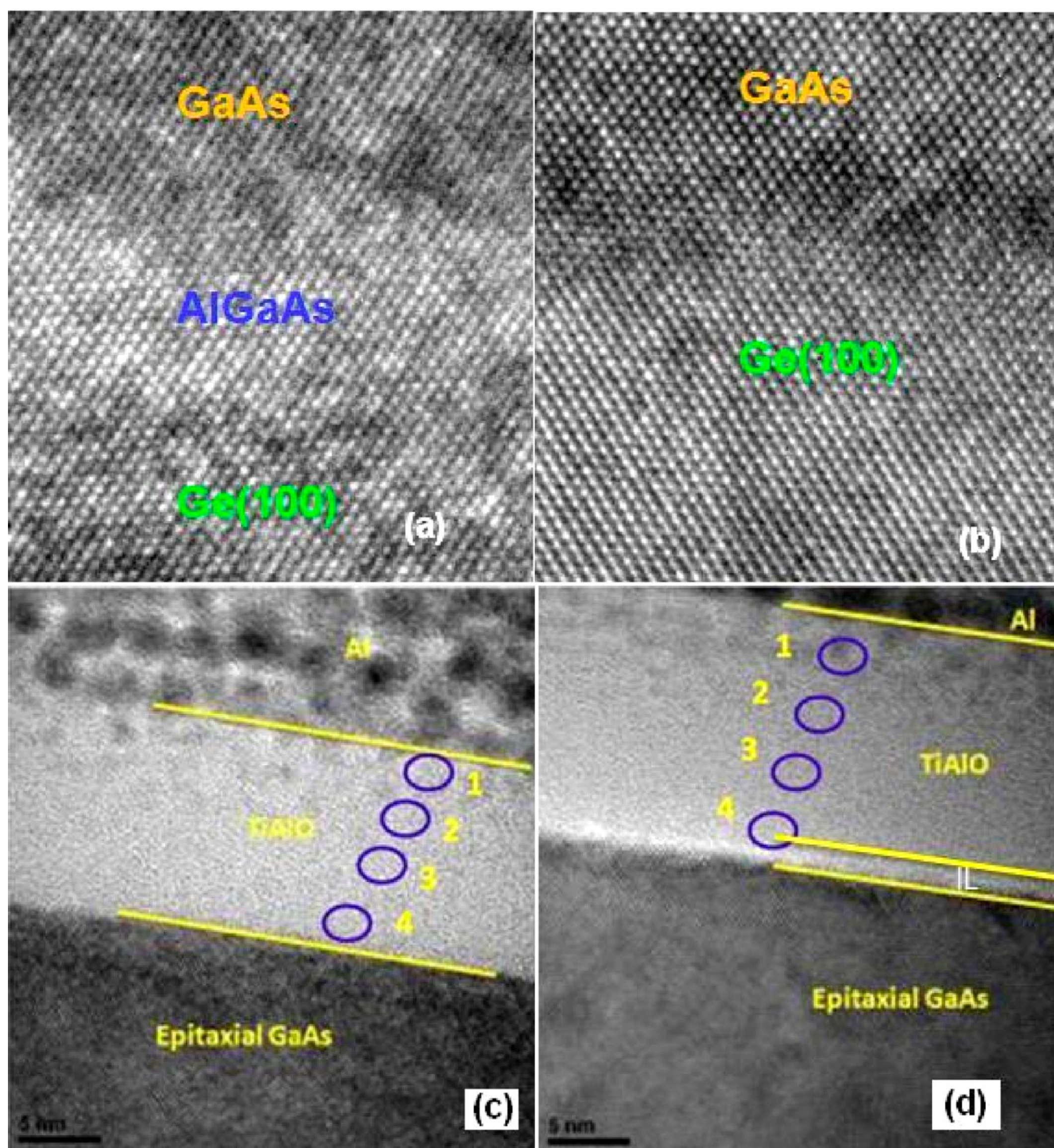

Figure 2. High resolution TEM at (a) GaAs/AlGaAs/Ge interface and (b) GaAs/Ge interface. Cross-sectional HRTEM of (c) Al/TiAlO/epi-GaAs/AlGaAs/Ge and (d) Al/TiAlO/epi-GaAs/Ge MOS structure. Atomic concentration of Ga, As, and Ge was calculated by using EDX analysis. The numbers correspond to each beam position for the EDX analysis.

■ RESULTS AND DISCUSSION

The surface roughness of epi-GaAs and bulk p-GaAs was measured using atomic force microscopy (AFM). The surface topography of epi-GaAs/Ge is nonuniform; it varies with the scan areas. Figure 1a shows the surface topography of epi-GaAs over the area of 10×10 μm^2. The root-mean-square (rms) surface roughness is high, and the value is ~6 nm with a distinct triangular feature. These triangular features are typical of epi-GaAs grown directly on Ge(100) substrates with 6° off-cut toward the ⟨111⟩ direction. On a closer look with the scan area of 1×1 μm^2 (not shown), the surface roughness of epi-GaAs has a lower value compared with the large area (10×10 μm^2). This suggests that the epi-GaAs has nonuniform surface topography, which also leads high surface roughness of ALD coated TiAlO on the epi-GaAs layer. The surface roughness for ALD coated TiAlO on the epi-GaAs layer was found to be in the range of ~6.6−7.2 nm over the scan area of 10×10 μm^2 (Figure 1b,c). On the other hand, the epi-GaAs layers with AlGaAs buffer layers reveals excellent surface morphology with low rms roughness of ~0.68 nm over the scan area of 1×1 μm^2, and the rms value remains same over the large area. Moreover, the surface roughness varies slightly between 0.65 to 0.71 nm with ALD coated TiAlO dielectric (Figure 1d−f). It is worthwhile to note that the surface morphology for epi-GaAs with AlGaAs buffer layer is comparable with bulk-GaAs substrates. The TiAlO dielectric on bulk p-GaAs substrate shows rms roughness of 0.23 −0.30 nm (Figure 1g−i). The surface roughness of bulk-GaAs with ALD coated TiAlO is very low, and the value is typically observed for Si based MOS devices. Furthermore, this rms value is lower compared with the reported results on ALD Al_2O_3 deposited on similar chemically treated bulk-GaAs substrates.[12] Low surface roughness of TiAlO on epi-GaAs with AlGaAs buffer layers reveals better surface morphology compared with epi-GaAs directly grown on Ge substrates. This is due to the strain compensation at the GaAs/AlGaAs interface and AlGaAs/Ge interfaces.[17] The smooth and uniform surface morphology of epi-GaAs layers

with AlGaAs buffer layer provides a platform to integrate high-*k* dielectrics for epi-GaAs/Ge based device application. The epi-GaAs/Ge based device requires high quality interface between high-*k* dielectric and epi-GaAs layers. Generally, the interface quality depends on the surface morphology of the starting layers. To the best of our knowledge, by using ALD TiAlO dielectric and epi-GaAs with AlGaAs buffer layer, we have achieved uniform films with lowest surface roughness for epi-GaAs based gate stacks. Moreover, that the surface roughness of TiAlO continues to remain the same even upon annealing reveals good thermal stability of the TiAlO/epi-GaAs/AlGaAs/Ge stacks.

The high resolution transmission electron microscopy (HRTEM) analysis is performed to investigate the interface properties and TiAlO dielectric quality on epi-GaAs layers with and without AlGaAs buffer layers. The ALD TiAlO dielectric was deposited on high quality epi-GaAs layer. The epi-GaAs layer was grown on Ge substrate with AlGaAs and without AlGaAs buffer layer, as shown in Figure 2a,b, respectively. The corresponding high-resolution TEM images at the interface between TiAlO and the epi-GaAs layer are shown in Figure 2c,d. For TiAlO/epi-GaAs/AlGaAs/Ge structure, the thickness of TiAlO is ~14 nm as shown in Figure 2c, which increased to 15.5 nm for TiAlO/epi-GaAs/Ge due to higher surface roughness of the epi-GaAs layers grown directly on Ge substrates without any buffer layer. According to Kim et al.[25] the growth rate in ALD processes strongly depends on the density of functional groups on the reaction surface. It has been confirmed from the experiments that the saturated density of functional groups on the semiconductor reaction surface is changed during ALD growth. Thus, due to higher surface roughness, epi-GaAs exhibited a higher density of surface hydroxyl groups which further enhance the film thickness of TiAlO dielectric.[12,25] Thus for the scale device, it is necessary to reduce the surface roughness of the epi-GaAs layer.

A clear and sharp interface between TiAlO and epi-GaAs layers was observed for the epi-GaAs with AlGaAs buffer layer, as shown in Figure 2c,d, respectively. According to the HRTEM images, the TiAlO film is amorphous in nature even after annealing at 500 °C. This is due to the presence of Al_2O_3 in TiO_2 films, which retains a high permittivity close to that of TiO_2 and also has excellent thermal stability like that of Al_2O_3.[20] From the line energy dispersive X-ray analysis for the alloy gate stacks, the atomic concentration of Al and Ti is found to be ~28% and 21%, respectively. The incorporation of elemental Ga and As into the dielectric is believed to be responsible for the degradation of electrical properties of the MOS device.[6,18] Therefore, the out-diffused elemental atoms are also a major concern for the reliability of the device. The interface quality as well as dielectric quality degrades due to the traps created by the out-diffusion of the elemental Ga and As atoms. The percentile amount of elemental Ga and As at different positions of TiAlO dielectric is measured by EDX analysis. The result shows that a very low amount of Ga diffuses into the dielectric. There is almost no presence of elemental As in the dielectric. Thus, TiAlO dielectric is able to reduce the out-diffusion of elemental Ga and As. This is due to the Ti incorporation into Al_2O_3, which acts as a barrier to elemental diffusion of Ga and As into the dielectric.[23]The amount of elemental Ga present in the TiAlO dielectric is also much lower compared with the alloy dielectric of HfO_2 and Al_2O_3 (HfAlO) deposited on the p-GaAs substrates.[6] It is worth noting that the percentile amount of Ga and As decreases further with the presence of thin AlGaAs buffer layers for the epi-GaAs layer, as shown in Table 1. The ALD TiAlO dielectric not only improves the interface quality by reducing the formation of defective native oxides (gallium-arsenide oxide) but also reduces the out-diffusion of elemental Ga and As, which are mainly responsible for increase oxide trap charges in the dielectric. Thin IL between TiAlO and the epi-GaAs layer (1.2 nm) was observed where epi-GaAs was grown directly on Ge substrates. On the other hand, there is no distinguishable IL between TiAlO and the epi-GaAs interface, where epi-GaAs was grown on Ge substrates with AlGaAs buffer layer. The combination of TiAlO dielectric and epi-GaAs with AlGaAs buffer layer plays a crucial role to suppress the out-diffusion of elemental atoms into the dielectric, which mainly degrades electrical performance of the devices.

Table 1. Amount of Out-Diffused Ga and As into the TiAlO Dielectric after PDA at 500 °C

	TiAlO/epi-GaAs/Ge		TiAlO/epi-GaAs/AlGaAs/Ge	
EDX positions	Ga (%)	As (%)	Ga (%)	As (%)
1	0.0	0	0.4	0.29
2	4.4	0	1.92	0.29
3	5.94	0	2.01	0.31
4	8.64	1.03	5.96	2.25

The interface chemical state of the ALD TiAlO alloy dielectric on epi-GaAs and bulk-GaAs sample was analyzed by XPS using a VG ESCALAB 220i-XL XPS system with monochromatic Al Kα source (1486.6 eV). Figure 3a−c illustrates the O 2s and Ga 3d spectra of different epi-GaAs with and without AlGaAs interlayer in comparison with the bulk GaAs after TiAlO deposition. The Ga 3d core level peak for the substrate was placed at 19.2 eV, and the chemical shifts used were +1 eV for the Ga^{1+} (Ga_2O) component and +1.8 eV for the Ga^{2+} (GaO) state.[26−28] The O 2s spectrum consists of the following two peaks: Ga−O−Ti and Ga−O−Al bonds at 23

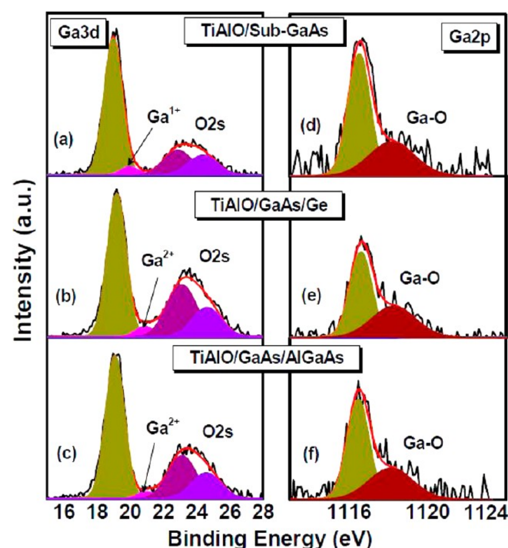

Figure 3. XPS core-level spectra of (a) Ga 3d and (d) Ga 2p from TiAlO/bulk p-GaAs, (b and e) TiAlO/epi-GaAs/AlGaAs/Ge, respectively, and (c and f) TiAlO/epi-GaAs/Ge structures after annealing at 500 °C in N_2 for 1 min, respectively.

eV and 24.5 eV attributed to formation of mix bonding in the interface. As the electron affinity of Al is quit higher that of Ti, we have assumed that the higher O 2s peak is related with Al−O−Ga. The O 2s spectra of these samples are close to the previous reported results.[29] From the Ga 3d spectrum it is evident that the Ga−O feature has multiple oxidation states for different samples including Ga^{1+} and Ga^{2+} probably due to Ga_2O and GaO formation. It is important to note that the TiAlO deposition has resulted in a Ga−O peak that is centered at a lower binding energy for bulk GaAs samples. But for epi-GaAs/AlGaAs/Ge and epi-GaAs/Ge the resulting Ga−O feature with low intensity presents in the higher energy position. According to Hinkle et al.[30] binding energy may shift due to charge redistribution from second nearest neighbor changes in the Ga−O bonding environment. In our previous study, we have also found that there was a very thin interfacial layer of Ga_2O on the surface of bulk-GaAs for ALD HfO_2; however, for epi-GaAs with high surface roughness (∼5 nm), the interface is distorted and shows a higher oxidation state of Ga, which is more closely related to the interface defects formation.[14,26] Suppressing the formation of Ga_2O_x native oxide at the interface is important for epi-GaAs based devices to improve the interface quality. The formation of Ga_2O_x native oxide is also due to the intrinsic nature of n-type GaAs substrate.[6] Therefore, it is possible to suppress the formation of Ga_2O_x native oxide at the interface by using p-type epi-GaAs layer with smooth surface morphology.

Accurate identification of the 2p peak is more important, since these peaks represent smaller sampling depths and, hence, are more sensitive to surface modification than 3d peaks. Second Ga 2p peaks have the highest intensities in XPS of GaAs. So statistically it has more accurate identification of the peaks in a shorter collection time. From Figure 3d−f, the bulk Ga 2p peak was found at 1116.6 eV. According to the Ga 2p spectra, the IL intensity is higher compared to the epi-GaAs layer; however, the peak position is at lower energy compared with epi-GaAs layer, which suggests the formation of stable native oxide for bulk-GaAs surface. For epi-GaAs with AlGaAs buffer layer, the intensity is lower compared with epi-GaAs without any buffer layer. Careful analysis shows that the Ga 2p peak position has also slightly lower energy compared with epi-GaAs without buffer layer. The higher oxidation states are more related with interface defects.[26] Thus, by introducing the AlGaAs buffer layer, it is possible to reduce Ga−O formation and improve the interface quality. The reduction of Ga−O formation is due to the surface roughness that was modified by introducing the AlGaAs buffer layer. Therefore, it can be concluded that the surface roughness is one of the key determining factors for the interfacial growth on epi-GaAs as seen from the XPS and HRTEM analysis. The improvement of surface passivation on the GaAs layer by using TiAlO dielectric was also observed from the analysis of the As 3d spectra. Figure 4 shows the As 3d spectra for TiAlO dielectric deposited on epi-GaAs and bulk-GaAs after annealing at 500 °C. There were no detectable arsenic oxides at the interface for bulk-GaAs substrates as well as for epi-GaAs layers, which suggests the importance of TiAlO dielectric for surface passivation on GaAs layers.

The presence of a thick interfacial layer for the bulk-GaAs substrate is also observed in SIMS analysis. The IL and interdiffusion of elemental atoms at the interface of TiAlO/epi-GaAs were studied using time-of-flight SIMS (TOFSIMS) analysis. Figure 5a−c shows the depth profiles of Ga and As at

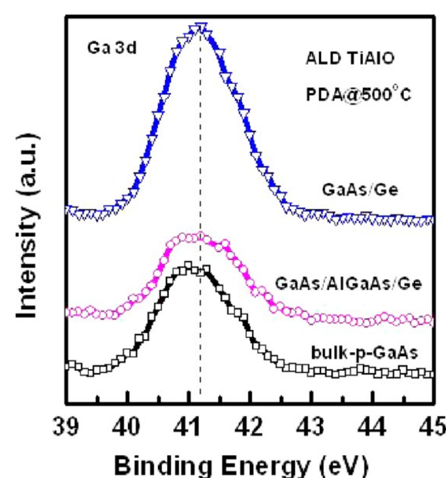

Figure 4. XPS of As 3d for TiAlO dielectric deposited on epi-GaAs layer and bulk-GaAs substrates.

the interface of TiAlO and GaAs. The presence of a Ga rich region was observed in the TiAlO film directly above the interfacial oxide. In the case of bulk-GaAs, it is found that Ga concentration is higher than the epi-GaAs. This is also in good agreement with XPS analysis, where we observed formation of stable Ga_2O on bulk-GaAs. On the other hand, for the epi-GaAs layer, there is Ga−O−Ti or Ga−O−Al related species present at the interface. According to the EDX analysis, Ga diffusion happens during thermal treatment of TiAlO dielectric and forms the TiGaO or AlGaO layer at the interface. It is also worth noting that there was no detectable As in the dielectric, which suggested the complete suppression of elemental As into the dielectric.

The impacts of elemental out-diffusion on the electrical properties of GaAs metal oxide semiconductor capacitors (MOSCs) have been studied by using capacitance−voltage ($C-V$) and current−voltage ($I-V$) characteristics. GaAs-MOSCs were fabricated on bulk-GaAs and epi-GaAs layers using aluminum (Al) as a gate electrode (area: 2.5×10^{-4} cm^2). Low resistance Ohmic back contact was formed by depositing Au on the back side of reference p-GaAs substrate and p-Ge substrate. Figure 6 shows the schematic diagram of MOSCs. The quality of TiAlO dielectric on the bulk-GaAs and epi-GaAs layer has been studied by measuring the hysteresis voltage in $C-V$ characteristics. Hysteresis voltage was determined by sweeping the gate voltage from inversion to accumulation and then sweeping back to obtain the difference of the flat-band voltage. This phenomenon is believed to be due to the presence of interfacial electrons and/or mobile charge in the oxide. For the GaAs based devices, it is observed due to the presence of elemental Ga and As into the dielectric. The hysteresis voltage in $C-V$ characteristics is found to be ∼5−10 mV for all the gate stacks as shown in Figure 7, which is excellent for the GaAs/TiAlO high-k gate stack. It is worth noting that the ALD TiAlO is deposited without any surface passivation layer and the hysteresis voltage is ∼5−10 mV for all the TiAlO/GaAs gate stacks with physical thickness of ∼14 nm. The hysteresis voltage in the $C-V$ curve for bulk GaAs MOSC is ∼5 mV. Even though directly deposited TiO_2 dielectric can reduce the hysteresis voltage, leakage current is too high due to insufficient conduction band offset.[10,31] Moreover, for directly deposited TiO_2, there is a presence of thick defective interfacial layer, which degrades interface quality.[10] On the other hand, ALD

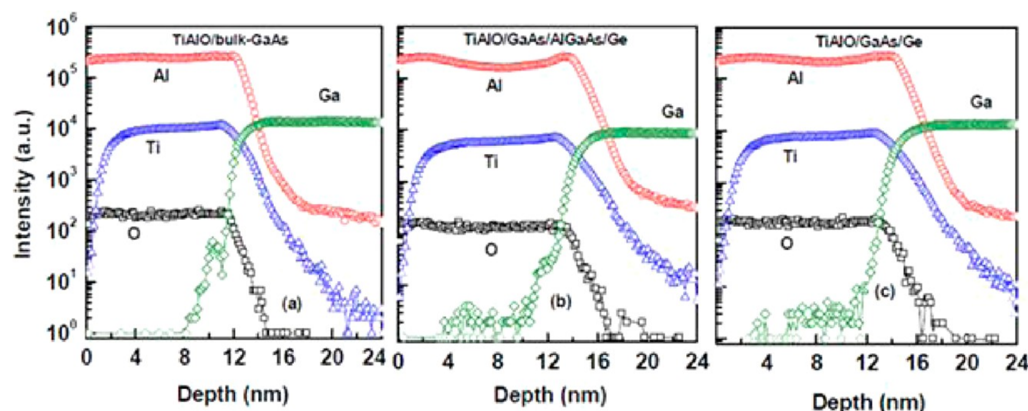

Figure 5. Experimental TOF−SIMS depth profiles obtained with Ar ions for interface of (a) TiAlO/sub-GaAs, (b) TiAlO/epi-GaAs/AlGaAs/Ge, and (c) TiAlO/epi-GaAs/Ge structures after annealing at 500 °C in N_2 for 1 min.

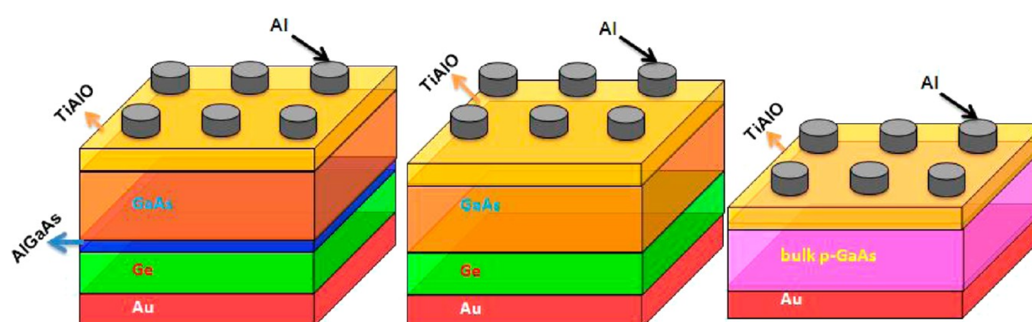

Figure 6. Schematic diagram of GaAs MOS capacitors fabricated on epi-GaAs with and without AlGaAs buffer layer and bulk-GaAs substrates.

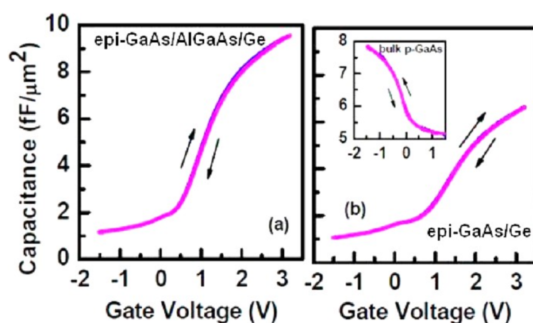

Figure 7. Hysteresis characteristics of epi-GaAs MOSC with (a) AlGaAs buffer layer and (b) without AlGaAs buffer layer. Inset of (a) shows hysteresis characteristic for bulk-GaAs substrate.

TiAlO alloy dielectric reduces hysteresis voltage without sacrificing the leakage current and interface quality. In our recent work for the TiAlO/InGaAs system, we found that the conduction band offset (CBO) is higher than 1 eV (CBO: 1.25 eV for TiAlO/InGaAs system).[23] Thus ALD TiAlO alloy dielectric is providing high quality surface passivation on the GaAs layer with low hysteresis voltage and high CBO. The effective dielectric constant (k_{eff}) of TiAlO was calculated from the $C-V$ characteristics using the equation $k_{eff} = Cd/\varepsilon_0$, where C is the accumulation capacitance per unit area, d is the total physical thickness of the gate stack (thickness of TiAlO dielectric and interfacial layer), and ε_0 is the free space permittivity. Table 2 compares the hysteresis voltage and effective dielectric constant of TiAlO alloy dielectric with other high-k dielectrics deposited on GaAs substrate and epi-GaAs layer. It shows that the TiAlO dielectric is able to provide significantly high effective dielectric constant with very low hysteresis voltage on bulk GaAs substrates and epi-GaAs layer.

Table 2. Comparison of Dielectric Thickness ($T_{high\text{-}k}$), Equivalent Oxide Thickness (EOT), Effective Dielectric Constant (k_{eff}), and Hysteresis Voltage (ΔV_{FB}) of TiAlO Dielectric with Different High-k Dielectrics Deposited on Bulk-GaAs Substrates and epi-GaAs Layer Using Atomic Layer Deposition (ALD) and Physical Vapor Deposition (PVD) Techniques

substrate	deposition and dielectric	$T_{high\text{-}k}$ (nm)	EOT (nm)	k_{eff}	ΔV_{FB} (mV)	refs
p-GaAs	ALD Al_2O_3	5		6.2	200	12
p-GaAs	ALD Al_2O_3	10		7.6	400	12
p-GaAs	ALD HfAlO	6.2	3.2	7.5	600	6
p-GaAs	ALD HfO_2	7.2	3.2	8.7	400	6
p-GaAs	ALD TiAlO	13	4.1	14	5	this work
n-GaAs	ALD HfO_2	7.2	3.2	8.8	1200	6
n-GaAs	ALD AlN/HfO_2	2/35	11	13		33
n-GaAs	PVD Si/PVDHfO$_2$	2.4/11			400	8
p-InGaAs/InP	ALD TiAlO	13	3.4	19	90	23
Epi-GaAs/Ge	ALD HfO_2	6.2	1.4	15	720	14
Epi-GaAs/Ge	ALD TiAlO	15.3	4.7	13	10	this work
Epi-GaAs/AlGaAs/Ge	ALD TiAlO	14	3.2	17	10	this work

To understand the formation of interfacial layer in detail, we have simulated $C-V$ characteristic using SILVACO, a commercially available software package, and compared with

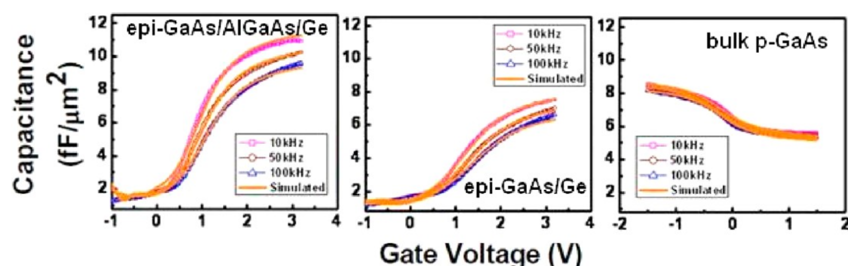

Figure 8. Capacitance−voltage ($C-V$) characteristics of (a) epi-GaAs MOSC with AlGaAs buffer layer, (b) epi-GaAs MOSC without AlGaAs buffer layer, and (c) for bulk p-GaAs MOSC measured at different frequencies and compared with simulated $C-V$ characteristics.

experimental results. For simulation, the virtual identical MOS structures are fabricated following the similar process recipe as that of the current experiment. The simulated $C-V$ curves are fitted excellently with the experimental data, as shown in Figure 8. To model the $C-V$ characteristics, an interfacial layer of thickness ∼0.7−2.2 nm has been incorporated during simulation. The IL thicknesses for epi-GaAs are 0.8 and 1.2 nm, for the MOSC with AlGaAs and without any buffer layer, respectively. The interfacial layer thickness for the bulk p-GaAs based MOS device of 2.2 nm was obtained from the simulation of $C-V$ characteristics. This is a good agreement with XPS and SIMS results that there is a formation of thick stable Ga_2O interfacial layer between bulk p-GaAs and TiAlO dielectric. From the simulation of $C-V$ characteristics, it is also observed that the dielectric constant of interfacial layer on bulk-GaAs substrate is higher than that of the epi-GaAs layer (Table 3).

Table 3. Doping Concentration of Substrates (n), Thickness of TiAlO Dielectric (d_{TiAlO}), Dielectric Constant of TiAlO (K_{TiAlO}), Interfacial Layer Thickness (d_{IL}), and Dielectric Constant of IL (K_{IL}) Used for the Simulation[a]

substrates	n (/cm^3)	d_{TiAlO} (nm)	K_{TiAlO}	d_{IL} (nm)	K_{IL}
Epi-GaAs/AlGaAs/Ge	2.8×10^{17}	14	24	0.8	5
Epi-GaAs/Ge	4×10^{18}	15.5	24	1.2	4
bulk p-GaAs	2×10^{18}	13	24	2.2	7.3

[a]The doping concentration of the bulk GaAs and epi-GaAs layer are chosen from ref 24.

This reveals the formation of a stable interfacial layer on bulk-GaAs substrate. On the other hand, even though the interfacial layer thickness for the epi-GaAs MOS device is thinner than that of the bulk GaAs, the frequency dispersion is much higher compared with that of bulk GaAs-MOSC, and this is due to the formation of interfacial gallium oxide (Ga_2O_x) with higher oxidation states than Ga_2O. Interfacial gallium oxides with higher oxidation states are more responsible to degrade the interfacial quality between GaAs and dielectric.[14,26]

Our separate evaluation of interface trap densities, measured using a conductance technique, also shows low interface trap defect density for bulk-GaAs MOSC with TiAlO dielectric. A conductance method is considered to be the most sensitive method for determining interface trap density (D_{it}). The peak conductance versus frequency [$G_p/\omega qA$ vs $\log(f)$] curves are shown in the gate voltage regime from +0.2 to +0.9 V at frequency range of 10−100 kHz. Figure 9a−c shows the maximum value of the $G_p/\omega qA$ peaks was measured at 30 kHz. Therefore 30 kHz was chosen as the measurement frequency for the interface trap calculation. The D_{it} can be estimated using the equation $D_{it} = (0.4 \times G_p/\omega)/qA$, where G_p is the peak conductance.[32] D_{it} calculated for TiAlO/epi-GaAs/AlGaAs/Ge and TiAlO/epi-GaAs/Ge at the midgap was estimated to be $\sim 6 \times 10^{11}$ cm^{-2} eV^{-1} for bulk GaAs based devices. The D_{it} values are $\sim 1 \times 10^{12}$ and $\sim 3 \times 10^{12}$ cm^{-2} eV^{-1} for the epi-GaAs based device with AlGaAs buffer layer and without buffer layer, respectively. The extracted values of D_{it} are comparable to the reported results for high-k dielectrics on bulk GaAs based devices.[18,33,34] The $G_p/\omega qA$ peak shift indicates that the surface potential responds efficiently to the gate bias when the Fermi level is located between conduction band edge and midgap for n-type epi-GaAs. Change in the ac-G peak indicates that the trapping at interface states dominates the trap kinetics at low oxide fields.[32] Therefore, we have also extracted D_{it} using the Terman method.[35] Figure 10 shows variation of D_{it} with energy. From Figure 10, it is noticed that the D_{it} at midgap is higher for the Terman method[35] compared to conductance method. This is possible due to the larger band bending in case of the Terman method compared with the conductance method. The overestimation of band bending due to the slow charge trapping/detrapping by the Terman method gives higher D_{it}. The interface trap density determined by the

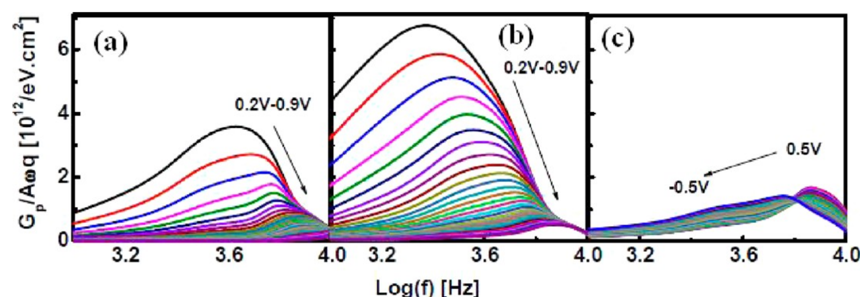

Figure 9. G_p/Awq vs $\log(f)$ characteristics of Al/TiAlO/GaAs MOS capacitors for epi-GaAs with AlGaAs buffer layer (a),without AlGaAs buffer layer (b), and for bulk p-GaAs substrate (c).

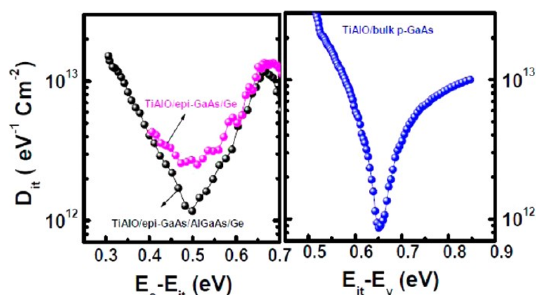

Figure 10. D_{it} spectra with energy for epi-GaAs MOSC and bulk-GaAs MOSC. D_{it} was calculated using the Terman method.

conductance method only deals with fast interface traps with short response times. However, for the Terman method, both fast and slow traps are taken into consideration, which gives higher value compared with conductance method.[32]

Current−voltage (I−V) characteristics were performed on GaAs MOS capacitors to evaluate the TiAlO gate dielectric quality on the GaAs surface. The leakage current analysis shows a breakdown field of ~3.3 MV/cm for TiAlO dielectric deposited on the bulk GaAs substrate and epi-GaAs layer. The leakage current density shown in Figure 11 is $\sim 5 \times 10^{-4}$ A/cm^2 at $V_{fb} + V$ with an EOT of ~3.2 nm for epi-GaAs with AlGaAs buffer layers. The leakage current is slightly high for an EOT of 3.2 nm. This is due to the lower band gap of the TiAlO dielectric.[23] The leakage current can be improved further by optimizing Ti concentration in the TiAlO dielectric, since the presence of Ti in Al_2O_3 decreases the band gap of the material. The conduction mechanism of the leakage current is similar to the Fowler−Nordheim (F−N) tunneling characteristics. F−N tunneling plot was performed as shown in the inset of Figure 11. A straight line was observed, which indicates the presence of an F−N tunneling phenomenon. Since F−N tunneling conduction requires sufficient band offsets and a low density of oxide traps in the dielectric, the presence of the F−N tunneling phenomenon reveals the high quality TiAlO dielectric on epi-GaAs and bulk-GaAs with sufficient band gap.

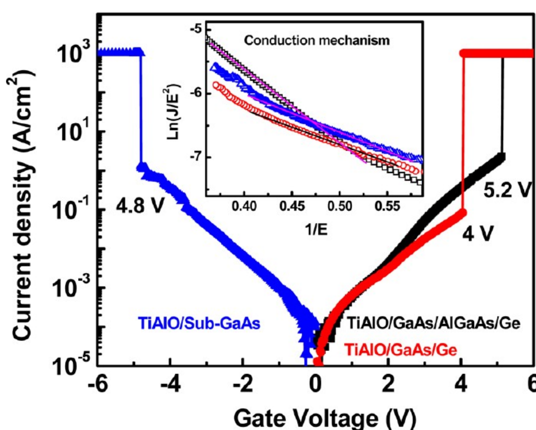

Figure 11. Leakage current density−voltage characteristics for ~14 nm TiAlO film on epi-GaAs as well as bulk GaAs substrate. The inset shows F−N fitting of leakage current for different gate stacks.

CONCLUSION

Surface passivation of bulk-GaAs and epi-GaAs layer with ALD TiAlO dielectric is demonstrated to yield a high quality interface between high-k dielectric and GaAs layer. The ALD TiAlO dielectric acts as an effective barrier to suppress the out-diffusion of elemental Ga and As into the dielectric. The ALD TiAlO eliminates formation of arsenic oxide completely from the GaAs surface. The stable Ga_2O interfacial layer was formed on the bulk-GaAs surface. Excellent electrical properties with low hysteresis voltage (5 mV) and interface defects (6×10^{11} eV^{-1} cm^{-2}) were observed for bulk-GaAs MOS capacitors. It has been also demonstrated that the TiAlO dielectric is a promising candidate for epi-GaAs based devices. By introduction of the thin AlGaAs buffer layer between epi-GaAs and Ge substrates, it is possible to improve the surface roughness of TiAlO/epi-GaAs gate stack and uniformity of the films, out-diffusion of elemental Ga into the dielectric, and interface quality between epi-GaAs and TiAlO dielectric further. The electrical characteristics of epi-GaAs MOSC with AlGaAs buffer layer shows higher accumulation capacitance, lower fixed oxide charge, and leakage current compared with epi-GaAs gate stack without buffer layer. The leakage current conduction mechanism shows the presence of F−N tunneling for the TiAlO dielectric with epi-GaAs and bulk-GaAs substrates. The results suggest that the high quality gate dielectric stacks on bulk-GaAs substrates and epi-GaAs layers with AlGaAs buffer layer can pave the way toward the next generation III−V/Si based high speed transistors.

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Notes

The authors declare no competing financial interest.

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